TECHNICAL NOTE



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SD12 - Changing worksurface Baud Rate for V1090+

In order to improve the performance of SD12 PC to worksurface communications, changes were made in the SD12 V1090+ application and the worksurface code was updated to V47.

With this combination of application and worksurface codes a change in the Baud Rate for the worksurface communications is critical for the system to function correctly.

The following notes describe how to make these Baud Rate adjustments after upgrading SD12 to V1090+

Upgrade the console software application in the normal way (refer to TN454 (Upgrading SD12 V1069-V1090).pdf.

When the upgrade is complete there is an option to run the upgrade hardware application, confirm this or access the same application from the Windows Start Menu as in the image below.



The following panel will be displayed:

daudara	de e estadore			and the later	an endered			Close
device	description	nie operati	running	available	required	update	F	
Engine	Host	SP6V.DIN	08/04/2019	08/04/2019		update	-	
	FPGA	SP6e.bit	29/01/2013	29/01/2013		update		engine serial number
	Effects	FX1.bin	18/04/2012	18/04/2012		update		00030176548732915394
	Host							
COM7	Host Interface	VulcanTiva.dfu	26	26		update		
	Host FPGA	Vulcan_Interface_FPGA.bit	22/02/2017	22/02/2017		update		
	USB Audio	xmos.bin		ОК		update		
	Surface							
COM4	SD12 Right	SD12worksurface.bin	39	47	 Image: A start of the start of	update		
сомз	SD12 Left	SD12worksurface.bin	39	47	 Image: A start of the start of	update		
COM5	SD12 Local IO	SD12LocalIO.hex	55	55		update		
COM6	SD12 GPIO	SD12GPIO.hex	10	10		update		
	DMI cards							
DMI 1	Firmware	digico_dmi.bin						
	FPGA							
DMI 2	Firmware	digico_dmi.bin						
	FPGA							
	Racks							
							1	
							1	
							1	
							1	
							1	
							1	
							1	

Click the "Update" button for "SD12 Right" – updating will start – wait for it to complete and then repeat the process for "SD12 Left"

		code versions					_	Cinee
device	description	file	running	available	required	update	-	01000
Ingine	Host	SP6v.bin	08/04/2019	08/04/2019		update		
	FPGA	SP6e.bit	29/01/2013	29/01/2013		update		
	Effects	FX1.bin	18/04/2012	18/04/2012		update		00030176548732915394
	Host							
COM7	Host Interface	VulcanTiva.dfu	26	26		update		
	Host FPGA	Vulcan_Interface_FPGA.bit	22/02/2017	22/02/2017		update		
	USB Audio	xmos.bin		ОК		update		
	Surface							
OM4	SD12 Right	SD12worksurface.bin	39	47		update		updating
сомз	SD12 Left	SD12worksurface.bin	39	47	 / 	update		SD12worksurface.bin
COM5	SD12 Local IO	SD12LocalIO.hex	55	55		update	1	to COM4
COM6	SD12 GPIO	SD12GPIO.hex	10	10		update	1	88
	DMI cards							packets sent
OMI 1	Firmware	digico_dmi.bin					1	
	FPGA						1	
OMI 2	Firmware	digico_dmi.bin					1	
	FPGA						1	
	Racks						1	
							1	

When both surfaces have been updated the panel should look like this – please note that it appears to still require an update – this is just a symptom of not having completed the following part of the process involving the change of Baud rate – see next step...

description Host FPGA Effects Host Host Interface Host FPGA USB Audio	code versions file SP6v bin SP6v bin SP6e bit FX1.bin VulcanTiva.dfu VulcanTiva.dfu	running 08/04/2019 29/01/2013 18/04/2012	available 08/04/2019 29/01/2013 18/04/2012	required	update update update	1	Close
description Host FPGA Effects Host Host Interface Host FPGA USB Audio	file SP6v.bin SP6e.bit FX1.bin VulcanTiva.dfu	running 08/04/2019 29/01/2013 18/04/2012	available 08/04/2019 29/01/2013 18/04/2012	required	update update update		
Host FPGA Effects Host Host Interface Host FPGA LISB Audio	SP8v.bin SP6e.bit FX1.bin VulcanTiva.dfu	08/04/2019 29/01/2013 18/04/2012	08/04/2019 29/01/2013 18/04/2012		update update		
FPGA Effects Host Host Interface Host FPGA LISB Audio	SP6e.bit FX1.bin VulcanTiva.dfu	29/01/2013 18/04/2012	29/01/2013 18/04/2012		update		
Effects Host Host Interface Host FPGA	FX1.bin VulcanTiva.dfu	18/04/2012	18/04/2012		undata		and a social south as
Host Host Interface Host FPGA	VulcanTiva.dfu	00			update		00030176548732915394
Host Interface Host FPGA	VulcanTiva.dfu	00					
Host FPGA		20	26		update		
USB Audio	vuican_interface_FPGA.bit	22/02/2017	22/02/2017		update		
000710000	xmos.bin		ок		update		
Surface							
SD12 Right	SD12worksurface.bin	39	47	 Image: A second s	update		updating
SD12 Left	SD12worksurface.bin	39	47	/	update		SD12worksurface.bin
SD12 Local IO	SD12LocalIO.hex	55	55		update		to COM3
SD12 GPIO	SD12GPIO.hex	10	10		update		undate successful
DMI cards							
Firmware	digico_dmi.bin						
FPGA							
Firmware	digico_dmi.bin						
FPGA							
Racks							
						1	
						-	
	Surface SD12 Right SD12 Lotal IO SD12 Lotal IO SD12 Cord IO SD12 GPIO DMI cards Firmware FPGA Firmware FPGA Racks to update	Surface SD12 Right SD12 Local SD12 GPIO	Surface Image: Surface bin 39 SD12 Lett SD12worksurface bin 39 SD12 Local IO SD12worksurface bin 39 SD12 Local IO SD12LocalOhex 55 SD12 GPIO SD12GPIO hex 10 DMI cards	Surface Surface Image: style styl	Surface Image: sector sec	Surface Image: series of the se	Surface Image: Surface bin series of the surface bin ser

If you close and reopen the update hardware application the panel will now appear like the image below and not indicate any "Running" surface code – don't worry about this – just proceed to the next step.

	-	Code Versions	1					Close
device	description	file	running	available	required	update	1-	
Engine	Host	SP6v.bin	08/04/2019	08/04/2019		update		
	FPGA	SP6e.bit	29/01/2013	29/01/2013		update		ongino porial number
	Effects	FX1.bin	18/04/2012	18/04/2012		update		00030176548732915394
	Host							
COM7	Host Interface	VulcanTiva.dfu	26	26		update		
	Host FPGA	Vulcan_Interface_FPGA.bit	22/02/2017	22/02/2017		update		
	USB Audio	xmos.bin		ОК		update		
	Surface							
COM4	SD12 Right	SD12worksurface.bin		47				
СОМЗ	SD12 Left	SD12worksurface.bin		47				
COM5	SD12 Local IO	SD12LocalIO.hex	55	55		update		
COM6	SD12 GPIO	SD12GPIO.hex	10	10		update		
	DMI cards							
DMI 1	Firmware	digico_dmi.bin						
	FPGA							
DMI 2	Firmware	digico_dmi.bin						
	FPGA							
	Racks							
							1	
							1	
							1	

Close the Update Hardware application.

From the Windows Start Bar, run the "SD12 Test" application as in the image below:



The application looks like the image below – click on the "Configure Ports" button in the top right corner of the panel.

SD12Test			
PiGiCo	5012 Se	erial Ports Display	Configure Ports RESET ALL
1: SD12 Right	2: SD12 Left	3: SD12 Local IO	4: SI)12 GPIO
Received: Button	Rotary Ro value Acce	Hardware ID 64 leration Code Version 39	Update Code (handshake off)
Send: LCD image	s single LCD All On Off	LEDs single on brightness	Calibrate Faders Calibrate Touch Brightness PSU bridge screen A: 12.1 V Temp B: LO V 26°C
Faders	Centre Deter	nt Backstop Ga	ing All h/phone level
		Send all Max Mia Mia Mia	periodic Jump Glide TT
54 172 58 228 128	50 52 210 50 228	30 74 180 18	speed 1000 ms
			×
Echo: Test		Single Echo Repeat	Echo All Ports

Another panel will open as below:

The Baud Rate or Ports 1 and 2 which should be set to 115200 must be changed to 256000 by typing into the relevant text boxes and then clicking OK at the bottom of the panel.

Config	ure Ports			×
	Ser	ial Po	orts	
	baud rate	enable	d com port	
All	115200	_		
1	115200 💌		4 VCP1	
2	115200 💌		3 VCP0	
3	102400 🔻		5 VCP2	
4	102400 💌		6 VCP3	
	🗸 ок		🗙 Cancel	
Config	ure Ports			X
connge	Seri	al Po	nts	
	baud rate e	enabled	com port	
All	115200 🔻			
1	256000 👻		4 VCP1 💌	1
2	256000 -		3 VCP0 -	i l
3	102400 👻		5 VCP2 -	
4	102400 💌		6 VCP3 👻	
		-		
	🗸 ок	1	Cancel	
		<u> </u>		

Now close the "SD12 Test" application shut down the console and power cycle.

When the SD12 application is running again, open the Master screen > System > Diagnostics Console tab and check the SD12 Right and SD12 Left "code" column entries now read **47** as in the image below.

Diagn	osiics						CLOSE
Console Engine Audio I/O Optocore Que	ies Logg	ing					
engine comms DK no errors engine 🏏	X	port	hardware	id	code		temp
surface comms OK optical comms OK midi IN OUT ••• average temperature 29 PSU: A 12V 12.1 B 12V LO	DO DO C IP address	0 1 2 3 4 5 6 7 8 9 10	SD12 Right SD12 Left SD12 Local IO SD12 GPIO	64 65 150 134	47 47 55 10	act act act act	30 28
Local I/O: 5V 5.0 +12V 11.9 48V 50 -12V 12.0 192.1	terface IP 168.8.53	11 12 13					
		14 15					